

Form 1449*	Atty. Docket No.: 303.390US3	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Joseph E. Geusic et al.	
	Filing Date: Herewith	Group: Unknown

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
<i>Self</i>	3,968,564	07/13/1976	Springthorpe, A.J.	29	580	04/30/75
<i>Self</i>	4,920,070	04/24/1990	Mukai, R.	437	173	11/27/87
<i>Self</i>	4,970,578	11/13/1990	Tong, E.K., et al.	357	81	09/28/88
<i>Self</i>	5,128,831	07/07/1992	Fox, III, A.C., et al.	361	396	10/31/91
<i>Self</i>	5,221,633	06/22/1993	Holm, P.M., et al.	437	51	09/09/91
<i>Self</i>	5,352,998	10/04/1994	Tamino, N.	333	247	10/01/93
<i>Self</i>	5,362,976	11/08/1994	Suzuki, K.	257	81	10/26/92
<i>Self</i>	5,409,563	04/25/1995	Cathey	156	643	02/26/93
<i>Self</i>	5,489,554	02/06/1996	Gates, J.L.	437	208	02/04/94
<i>Self</i>	5,532,506	07/02/1996	Tserng, H.Q.	257	276	11/14/94
<i>Self</i>	5,604,835	02/18/1997	Nakamura, T., et al.	385	129	12/22/94
<i>Self</i>	5,641,545	06/24/1997	Sandhu, G.S.	427	573	06/07/95
<i>Self</i>	5,656,548	08/12/1997	Zavracky, P.M., et al.	438	23	09/19/95
<i>Self</i>	5,682,062	10/28/1997	Gaul, S.J.	257	686	06/05/95
<i>Self</i>	5,729,038	03/17/1998	Young, W.R., et al.	257	460	12/15/95
<i>Self</i>	5,742,100	04/21/1998	Schroeder, J.A., et al.	257	778	03/27/95
<i>Self</i>	5,760,478	06/02/1998	Rozso, F.M., et al.	257	777	08/20/96
<i>Self</i>	5,767,001	06/16/1998	Bertagnolli, E., et al.	438	455	05/22/94
<i>Self</i>	5,798,297	08/25/1998	Winnerl, J., et al.	438	622	05/02/94
<i>Self</i>	5,834,849	11/10/1998	Lane, C.F.	257	786	02/13/96
<i>Self</i>	5,844,289	12/01/1998	Teranishi, N., et al.	257	432	05/21/97
<i>Self</i>	5,858,814	01/12/1999	Goossen, K.W., et al.	438	107	12/12/96
<i>Self</i>	5,897,333	04/27/1999	Goossen, K.W., et al.	438	455	03/14/97
<i>Self</i>	5,900,674	05/04/1999	Wojnarowski, R.J., et al.	257	774	12/23/96
<i>Self</i>	5,901,050	05/04/1999	Imai, R.	361	820	08/21/97
<i>Self</i>	5,902,118	05/11/1999	Hubner, H.	438	106	07/03/95
<i>Self</i>	5,903,045	05/11/1999	Bertin, C.L., et al.	257	621	04/30/96
<i>Self</i>	5,915,167	06/22/1999	Leedy, G.J.	438	108	04/04/97
<i>Self</i>	5,952,665	09/14/1999	Bhargava, R.N.	250	483.1	11/28/97

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**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
<i>Self</i>	03-013907	01/22/1991	Japan	G02B	6/12	
<i>Self</i>	04-263462	09/18/1992	Japan	H01L	25/04	
<i>Self</i>	05-145060	06/11/1993	Japan	H01L	29/44	
<i>Self</i>	91/11833	08/08/1991	PCT	H01R	9/00	
<i>Self</i>	94/05039	03/03/1994	PCT	H01L	23/48	

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No						

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

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JEV	Forbes, L., et al., "Resonant Forward-Biased Guard-Ring Diodes for Suppression of Substrate Noise in Mixed-Mode CMOS Circuits", <u>Electronics Letters</u> , 31, 720-721, (April 1995)
JEV	Foster, R., et al., "High Rate Low-Temperature Selective Tungsten", In: <u>Tungsten and Other Refractory Metals for VLSI Applications III</u> , V.A. Wells, ed., Materials Res. Soc., Pittsburgh, PA, 69-72, (1988)
JEV	Gong, S., et al., "Techniques for Reducing Switching Noise in High Speed Digital Systems", <u>Proceedings of the 8th Annual IEEE International ASIC Conference and Exhibit</u> , Austin, TX, 21-24, (1995)
JEV	Heavens, O., <u>Optical Properties of Thin Solid Films</u> , Dover Pubs. Inc., New York, 155-206, (1965)
JEV	Horie, H., et al., "Novel High Aspect Ratio Aluminum Plug for Logic/DRAM LSI's Using Polysilicon-Aluminum Substitute", <u>Technical Digest: IEEE International Electron Devices Meeting</u> , San Francisco, CA, 946-948, (1996)
JEV	Kim, Y.S., et al., "A Study on Pyrolysis DMEAA for Selective Deposition of Aluminum", In: <u>Advanced Metallization and Interconnect Systems for VLSI Applications in 1995</u> , R.C. Ellwanger, et al., (eds.), Materials Research Society, Pittsburgh, PA, 675-680, (1996)
JEV	Klaus, et al., "Atomic Layer Controlled Growth of SiO ₂ Films Using Binary Reaction Sequence Chemistry", <u>Applied Physics Lett.</u> 70(9), 1092-94, (3 March 1997)
JEV	Lehmann, et al., "A Novel Capacitor Technology Based on Porous Silicon", <u>Thin Solid Films</u> 276, Elsevier Science, 138-42, (1996)
JEV	Lehmann, V., "The Physics of Macropore Formation in Low Doped n-Type Silicon", <u>Journal of the Electrochemical Society</u> , 140(10), 2836-2843, (Oct. 1993)
JEV	Masu, K., et al., "Multilevel Metallization Based on Al CVD", <u>1996 IEEE Symposium on VLSI Technology, Digest of Technical Papers</u> , Honolulu, HI, 44-45, (June 11-13, 1996)

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03/17/2002

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feR	McCredie, B.D., et al., "Modeling, Measurement, and Simulation of Simultaneous Switching Noise", <u>IEEE Transactions on Components, Packaging, and Manufacturing Technology -- Part B</u> , 19, 461-472, (Aug. 1996)
feR	Muller, K., et al., "Trench Storage Node Technology for Gigabit DRAM Generations", <u>Digest IEEE International Electron Devices Meeting</u> , San Francisco, CA, 507-510, (Dec. 1996)
feR	Ohba, T., et al., "Evaluation on Selective Deposition of CVD W Films by Measurement of Surface Temperature", <u>In: Tungsten and Other Refractory Metals for VLSI Applications II</u> , Materials Research Society, Pittsburgh, PA, 59-66, (1987)
feR	Ohba, T., et al., "Selective Chemical Vapor Deposition of Tungsten Using Silane and Polysilane Reductions", <u>In: Tungsten and Other Refractory Metals for VLSI Applications IV</u> , Materials Research Society, Pittsburgh, PA, 17-25, (1989)
feR	Ott, A.W., et al., "Al3O3 Thin Film Growth on Si(100) Using Binary Reaction Sequence Chemistry", <u>Thin Solid Films</u> , Vol. 292, 135-44, (1997)
feR	Ramo, S., et al., <u>Fields and Waves in Communication Electronics</u> , Third Edition, John Wiley & Sons, Inc., pp. 428-433, (1994)
feR	Senthinathan, R., et al., "Reference Plane Parasitics Modeling and Their Contribution to the Power and Ground Path "Effective" Inductance as Seen by the Output Drivers", <u>IEEE Transactions on Microwave Theory and Techniques</u> , 42, 1765-1773, (Sep. 1994)
feR	Stanisic, B.R., et al., "Addressing Noise Decoupling in Mixed-Signal IC's: Power Distribution Design and Cell Customization", <u>IEEE Journal of Solid-State Circuits</u> , 30, 321-326, (Mar. 1995)
feR	Suntola, T., "Atomic Layer Epitaxy", <u>Handbook of Crystal Growth 3, Thin Films of Epitaxy, Part B: Growth Mechanics and Dynamics</u> , Elsevier, Amsterdam, 601-63, (1994)
feR	Sze, S.M., <u>VLSI Technology</u> , 2nd Edition, Mc Graw-Hill, NY, 90, (1988)

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<i>fell</i>	Vittal, A., et al., "Clock Skew Optimization for Ground Bounce Control", 1996 IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, San Jose, CA, 395-399, (Nov. 10-14, 1996)
<i>fell</i>	Wooley, et al., "Experimental Results and Modeling Techniques for Substrate Noise in Mixed Signal Integrated Circuits", IEEE Journal of Solid State Circuits, Vol SC-28, 420-30, (1993)

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